AMENDMENTS TO THE CLAIMS

1. (Original) A circuit comprising:

cache memory structure comprising multiple banks;

a plurality of access ports communicatively coupled to said cache memory structure;

circuitry operable to determine a bank conflict for pending access requests for said cache memory structure; and

circuitry operable to issue at least one access request to said cache memory structure out of the order in which it was requested, responsive to determination of said bank conflict.

2. (Original) The circuit of claim 1 wherein said bank conflict comprises a bank conflict between at least two access requests.

3. (Original) The circuit of claim 1 further comprising:

pending request queue to which said pending access requests for said cache memory structure are stored, wherein said bank conflict is determined for at least one pending access request upon entry of said at least one pending access request into said pending request queue.

4. (Original) The circuit of claim 3 wherein said bank conflict comprises a bank conflict between at least one pending access request and least one issued access request.

5. (Original) The circuit of claim 1 wherein said circuitry operable to issue at least one access request is further operable to issue said at least one access request according to a predefined pipeline, said predefined pipeline having a plurality of stages with one stage for performing a first type of access and a different stage for performing a second type of access.

6. (Original) The circuit of claim 5 wherein said bank conflict comprises a bank conflict between at least one access request of said first type with at least one access request of said second type.

7. (Original) The circuit of claim 5 wherein said first type of access request comprises a request for a data store operation to a particular bank of said cache memory structure, and wherein said second type of access request comprises a request for a data read operation to said particular bank of said cache memory structure.

8. (Original) The circuit of claim 5 wherein said pipeline comprises:

a stage for nominating non-conflicted access requests for issuance to said memory cache structure; and

another stage for issuing to said cache memory structure at least one nominated request.

9. (Original) The circuit of claim 1 wherein said bank conflict comprises a bank conflict between at least one of said pending access requests and an older access request.

10. (Original) The circuit of claim 1 further comprising:

pending request queue to which said pending access requests for said cache memory structure are stored, wherein said bank conflict comprises a bank conflict between sibling access requests that are inserted to said pending request queue in parallel and wherein said bank conflict between sibling access requests is determined upon entry of said sibling access requests into said pending request queue.

11. (Original) A method for resolving bank conflicts between access requests for a cache memory structure that comprises a plurality of address banks, said method comprising:

storing access requests for said cache memory structure to a pending request queue;

determining at least one access request in said pending request queue that has a bank conflict;

determining at least one access request in said pending request queue that does not have a bank conflict, wherein said determined at least one access request that does not have a bank conflict is newer than the determined access request that has a bank conflict; and

nominating at least the determined access request that does not have a bank conflict for issuance to said cache memory structure.

12. (Original) The method of claim 11 wherein said cache memory structure comprises a plurality of access ports, said method further comprising:

nominating a plurality of access requests that do not have bank conflicts for issuance to said cache memory structure.

13. (Original) The method of claim 12 further comprising:

issuing a plurality of nominated access requests to said cache memory structure in parallel via said plurality of access ports.

14. (Original) The method of claim 11 further comprising:

performing said step of determining at least one access request that has a bank conflict upon entry of said at least one access request that has a bank conflict to said pending request queue.

15. (Original) The method of claim 11 wherein said bank conflict comprises a bank conflict with an older request pending in said pending request queue.

16. (Original) The method of claim 11 wherein said at least one access request requests a first type of access, and wherein said bank conflict comprises a bank conflict between said at least one access request and at least one other access request requesting a different type of access.

17. (Original) The circuit of claim 16 further comprising:

issuing said at least one access request that does not have a bank conflict according to a predefined pipeline, said predefined pipeline having a plurality of stages with one stage for performing said first type of access and a different stage for performing said different type of access.

18. (Original) The circuit of claim 17 wherein said first type of access comprises a load from said cache memory structure, and wherein said different type of access comprises a store to said cache memory structure.

19. (Currently Amended) A computer system comprising:

memory structure comprising a plurality of address banks;

means for queuing access requests for said ~~cache~~ memory structure;

means for determining whether a bank conflict exists for a pending access request; and

means for nominating at least one pending access request for issuance to said ~~cache~~ memory structure, wherein responsive to said determining means determining that a bank conflict exists for a pending access request, said nominating means nominating at least one pending access request out of the order in which it was queued in said queuing means.

20. (Currently Amended) The computer system of claim ~~B1~~ 19 further comprising:

a plurality of access ports to said ~~cache~~ memory structure; and

means for issuing a plurality of nominated access requests to said ~~cache~~ memory structure in parallel via said plurality of access ports.